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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Pierre MARTY, Gaëlle REY and Pascal CHAUVET
Serial No.: 10/700,361
Filed: November 3, 2003
For: DRAM CONTROL CIRCUIT

Examiner: Unassigned
Art Unit: 2186

Confirmation No. 5357

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

- ☒ Request for Corrected Publication Pursuant to 37 CFR 1.221(b)
- ☒ Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 720-3500, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

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Attorney Docket No.: S1022.80985US01

Respectfully submitted,

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REQUEST FOR CORRECTED PUBLICATION PURSUANT TO 37 CFR 1.221(b)

Sir/Madam:

Applicants respectfully request correction of a material mistake, made in published patent application No. 2004/0210730 A1, published on October 21, 2004.

Specifically, Applicants note that on page 1, paragraph [0008] , line 14, use of the word “to” instead of the legend “t0” is incorrect. The legend “t0” is used to identify the time corresponding to the beginning of the first write request. However, in paragraph [0008], on line 14, where the word “to” has been substituted for the legend “t0” the sentence makes no sense.

Applicants wish to make this correction to the published application and accordingly enclose herewith a highlighted copy of page 2 of the application as filed. Page 2 shows that the text of the application as filed was not illegible. Page 2, line 21, of the specification reads as follows “At a time t1 occurring three periods T after time t0, block 10 provides bus ...”. Also enclosed is a highlighted copy of page 1 of published patent application No. 2004/0210730 A1, highlighting the corresponding text “At a time t1 occurring three periods T after time to, block 10 provides bus ...”.

Serial No.: 10/700,361
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- 2 -

Art Unit: 2186

Should any questions arise concerning the foregoing, the Examiner is invited to call the undersigned at the number listed below.

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XNDD

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Pierre Marty et al., Applicant

By: 

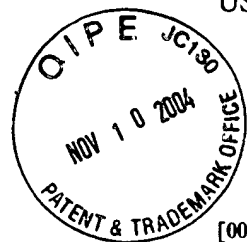
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initialization. Circuit 2 further includes a block 10, connected between the output of block 8 and bus COM, which converts the requests received by block 8 from a communication protocol specific to circuit 2 to a communication protocol specific to memory 4. The protocol accepted by a memory depends on the type and on the builder of the memory.

5 Fig. 2 schematically illustrates two series of instructions provided by block 10 at the rate of clock signal CK. In the example shown, block 10 receives a first request for writing a word, intended for an address A1' in a page A1 of memory area A, then a second request for writing a word, intended for an address B1' in a page B1 of memory area B. In the example shown, such write requests each start with the rewriting of the data of the considered cache
10 into a previously processed page (preload of the cache, instruction PRE), followed by the writing of the considered page into said cache (cache activation, instruction ACT), followed by the writing of the considered word into said cache (instruction WR).

At a time t0 corresponding to the beginning of the first write request, block 10 provides bus COM with an instruction PRE A0 for preloading cache BUFA. It should be
15 noted that the preload instruction is provided to cache BUFA in a period T of clock signal CK, but that a preload operation cannot be executed in one period only. The preload execution speed is a characteristic of memory 4. In the example shown, memory 4 executes the preload operation in three periods. Thus, during two periods following the reception of the preload instruction, the cache cannot receive other instructions and block 10 must provide
20 two non-instructions "NOP" between the preload instruction and the next activation instruction. At a time t1 occurring three periods T after time t0, block 10 provides bus COM with a page activation control signal ACT A1 requiring from cache BUFA to read the page of address A1 in memory area A. The activation instruction is provided to cache BUFA in one period T but the activation operation is executed in three periods, and block 10 needs to
25 provide two instructions NOP between the activation instruction and the next write instruction. At a time t2, occurring three periods T after time t1, block 10 provides an instruction WR A1' for writing the word having address A1' into cache BUFA. It should be noted that the word to be written at address A1' is provided to data bus DAT when instruction WR A1 is provided. A single period is necessary to execute the write operation. At a time t3
30 located one period T after time t2, the operation of writing the word of address A1' of page A1 into memory area A is over.

The second write request progresses in the same way as the first write request. At time



DRAM CONTROL CIRCUIT

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 10/406,627 filed on Apr. 3, 2003 which in turn is a continuation of U.S. application Ser. No. 10/111,506, filed on Apr. 23, 2002, entitled "Dram Control circuit," which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a memory control circuit, and in particular to a circuit for controlling an external memory of SDRAM, DDR, or RAMBUS type including several memory areas.

[0004] 2. Discussion of the Related Art

[0005] Many electronic systems must store a large amount of data in a memory and they must have fast access to these data. Memories of dynamic RAM or DRAM type, generally including several memory areas each accessible via a cache with a high data rate, are fit for this type of use. Such memories generally are discrete integrated circuits (external memories) which must be connected to memory control circuits for connection to the rest of the electronic system.

[0006] FIG. 1 schematically shows a memory control circuit 2 connected to a DRAM-type memory 4 via a control bus COM and a data bus DAT. Memory 4 includes two memory areas A and B, each of which is connected to data bus DAT via a cache, respectively BUFA and BUFB. Memory 4 is rated by a clock signal CK. Memory areas A and B are both organized in several memory pages (not shown), each of which includes a predetermined number of words. Caches BUFA and BUFB are connected by control bus COM to circuit 2. Circuit 2 includes a priority management block 8 connected to receive read and/or write requests from blocks (not shown), which are further connected to bus DAT to exchange data with memory 4. Block 8 receives write and/or read requests intended for one or the other of the memory areas. When block 8 simultaneously receives two requests provided by two blocks, it gives priority for processing to the request received from that of the two blocks holding the priority initialization. Circuit 2 further includes a block 10, connected between the output of block 8 and bus COM, which converts the requests received by block 8 from a communication protocol specific to circuit 2 to a communication protocol specific to memory 4. The protocol accepted by a memory depends on the type and on the builder of the memory.

[0007] FIG. 2 schematically illustrates two series of instructions provided by block 10 at the rate of clock signal CK. In the example shown, block 10 receives a first request for writing a word, intended for an address A1' in a page A1 of memory area A, then a second request for writing a word, intended for an address B1' in a page B1 of memory area B. In the example shown, such write requests each start with the rewriting of the data of the considered cache into a previously processed page (preload of the cache, instruction PRE), followed by the writing of the considered page into said cache (cache activation, instruction ACT), followed by the writing of the considered word into said cache (instruction WR).

[0008] At a time t0 corresponding to the beginning of the first write request, block 10 provides bus COM with an instruction PRE A0 for preloading cache BUFA. It should be noted that the preload instruction is provided to cache BUFA in a period T of clock signal CK, but that a preload operation cannot be executed in one period only. The preload execution speed is a characteristic of memory 4. In the example shown, memory 4 executes the preload operation in three periods. Thus, during two periods following the reception of the preload instruction, the cache cannot receive other instructions and block 10 must provide two non-instructions "NOP" between the preload instruction and the next activation instruction. At a time t1 occurring three periods T after time t0, block 10 provides bus COM with a page activation control signal ACT A1 requiring from cache BUFA to read the page of address A1 in memory area A. The activation instruction is provided to cache BUFA in one period T but the activation operation is executed in three periods, and block 10 needs to provide two instructions NOP between the activation instruction and the next write instruction. At a time t2, occurring three periods T after time t1, block 10 provides an instruction WR A1' for writing the word having address A1' into cache BUFA. It should be noted that the word to be written at address A1' is provided to data bus DAT when instruction WR A1 is provided. A single period is necessary to execute the write operation. At a time t3 located one period T after time t2, the operation of writing the word of address A1' of page A1 into memory area A is over.

[0009] The second write request progresses in the same way as the first write request. At time t3, block 10 provides an instruction PRE B0 for preloading cache BUFB. At a time t4 occurring three periods T after time t3, block 10 provides an instruction ACT B1 for activating the page of address B1 in memory area B. Finally, at a time t5 occurring three periods T after time t4, block 10 provides an instruction WR B1' for writing the word of address B1' of page B1.

[0010] It should be noted that when a first and a second write requests must be successively executed in a same page, the used cache already contains the right page after the first writing and it is not necessary to execute the second write request for block 10 to provide once again the instructions of preload and activation of said page. It should also be noted that some memories are provided to automatically have any writing into a word of a cache followed by a sequence of write operations into the following word of the cache. Such a writing sequence is called writing in burst mode. In a burst writing, the used cache cannot receive any other instruction and block 10 provides instructions NOP. A burst writing is conventionally interrupted by a predetermined instruction such as the preload instruction.

[0011] The execution of a request for reading a word from a page of the memory area is similar to the previously-described execution of a word write request, a word read instruction (RD) replacing the word write instruction (WR).

[0012] Recent technological progress has enabled developing DRAMs operating at very high frequencies ranging up to 800 MHz. It has up to now been possible to develop control circuits able to provide the control instructions of such memories, using particularly simple and fast architectures. However, the rate of data exchanged with the memory is desired to be further increased. It is possible to increase